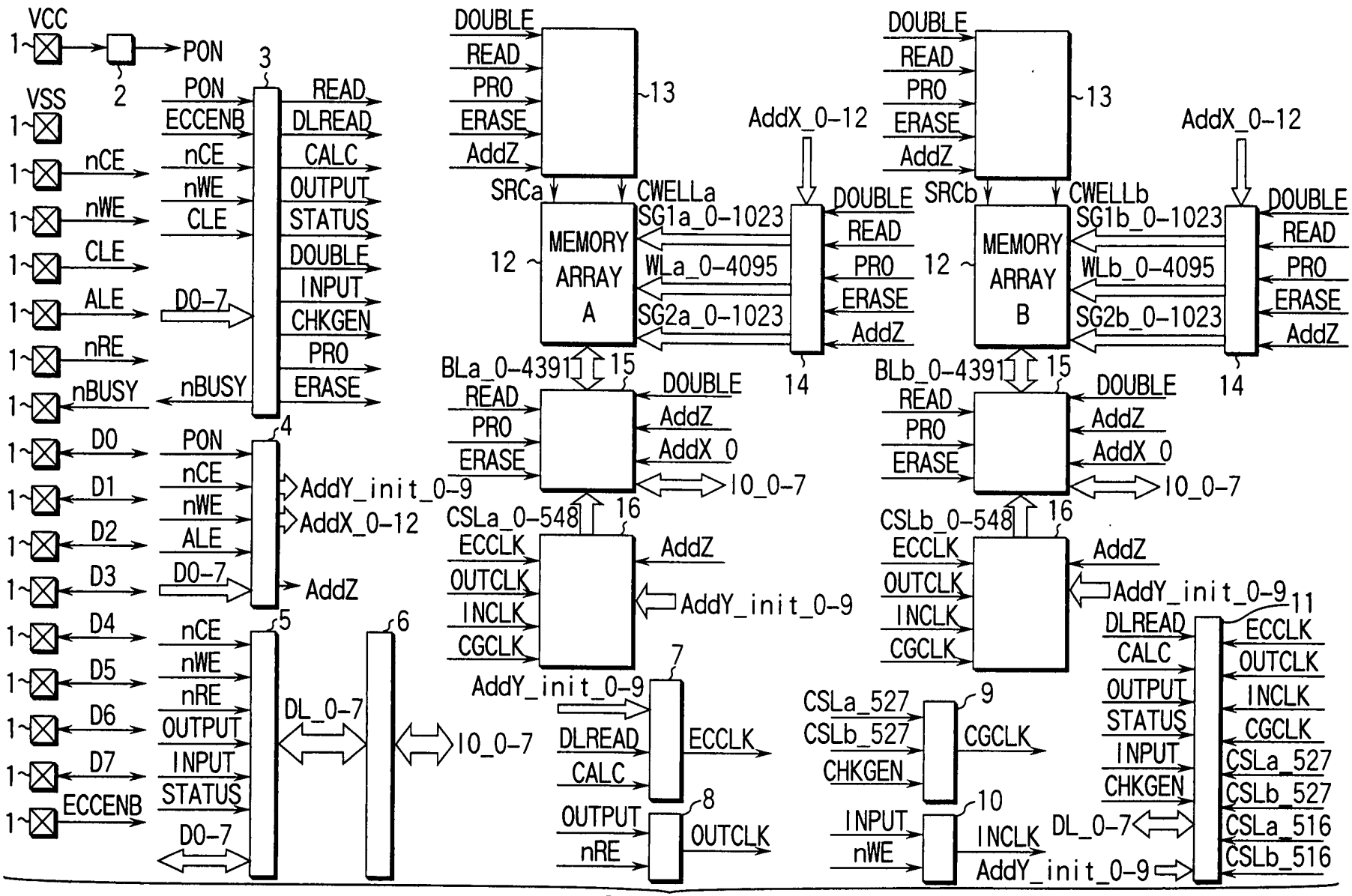

VCC
VSS
PON
nCE
nWE
CLE
ALE
nRE
nBUSY
D0
D1
D2
D3
D4
D5
D6
D7
ECCENB
D0-7
READ
DLREAD
CALC
OUTPUT
STATUS
DOUBLE
INPUT
CHKGEN
PRO
ERASE
AddY_init_0-9
AddX_0-12
AddZ
DL_0-7
IO_0-7
SRCa
CWELLa
SRCb
CWELLb
MEMORY ARRAY A
MEMORY ARRAY B
SG1a_0-1023
WLa_0-4095
SG2a_0-1023
SG1b_0-1023
WLb_0-4095
SG2b_0-1023
BLa_0-4391
BLb_0-4391
AddX_0
CSLa_0-548
CSLb_0-548
ECCLK
OUTCLK
INCLK
CGCLK
CSLa_527
CSLb_527
CSLa_516
CSLb_516
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

FIG. 1

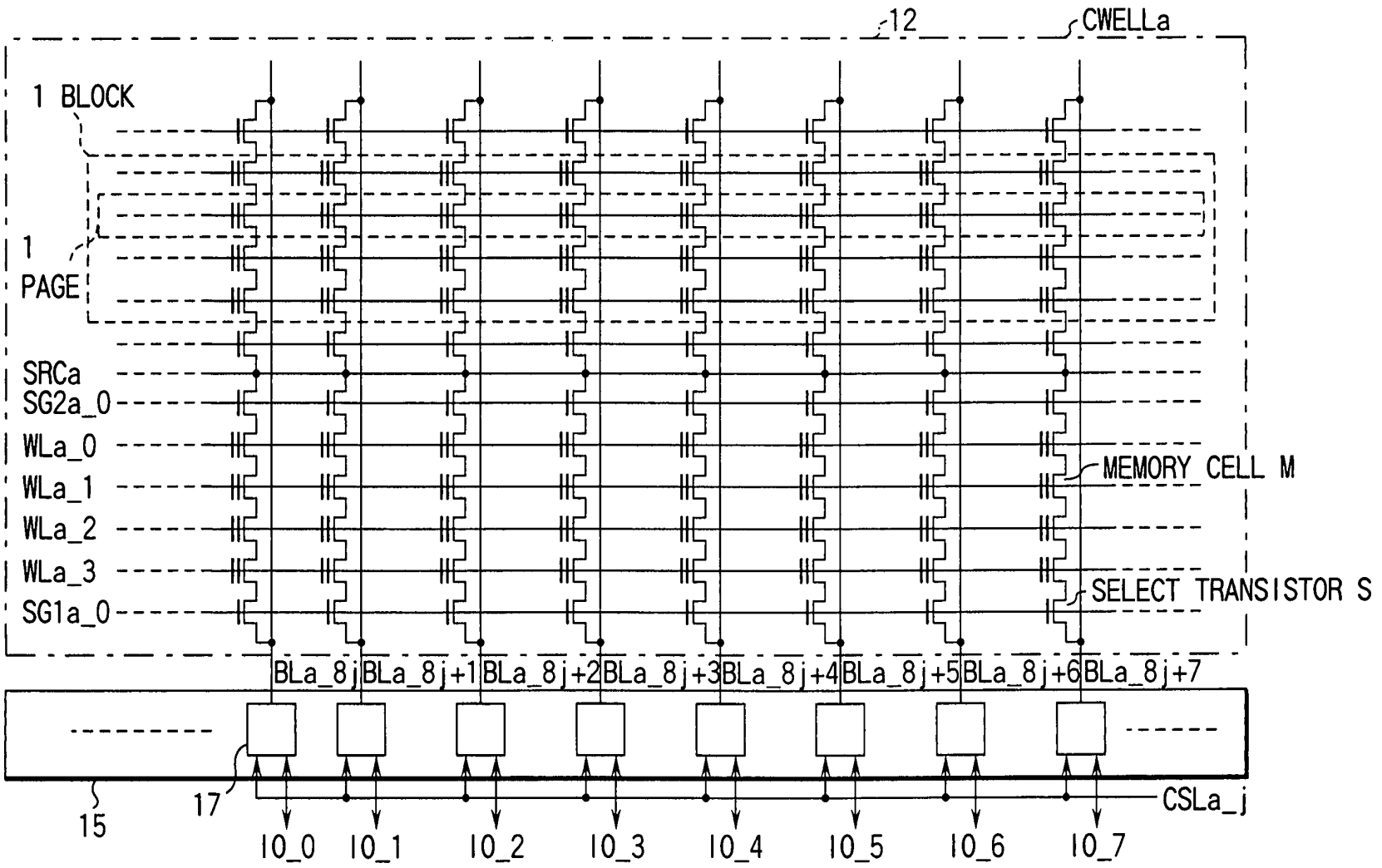

12
CWELLa
1 BLOCK
1
PAGE
SRCa
SG2a_0
WLa_0
WLa_1
WLa_2
WLa_3
SG1a_0
MEMORY CELL M
SELECT TRANSISTOR S
BLa_8j
BLa_8j+1
BLa_8j+2
BLa_8j+3
BLa_8j+4
BLa_8j+5
BLa_8j+6
BLa_8j+7
17
15
CSLa_j
IO_0
IO_1
IO_2
IO_3
IO_4
IO_5
IO_6
IO_7

FIG. 2

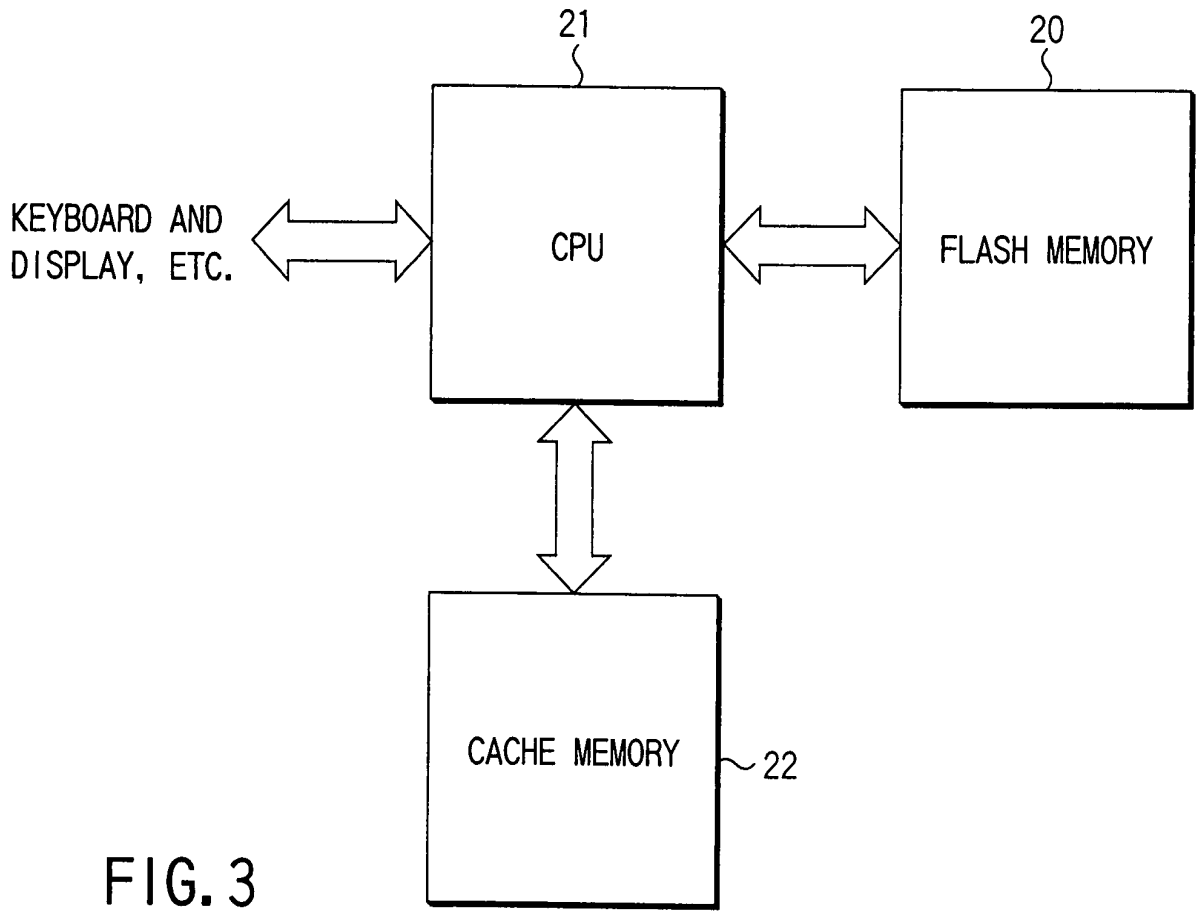

21
20
KEYBOARD AND
DISPLAY, ETC.
CPU
FLASH MEMORY
CACHE MEMORY
22

FIG. 3

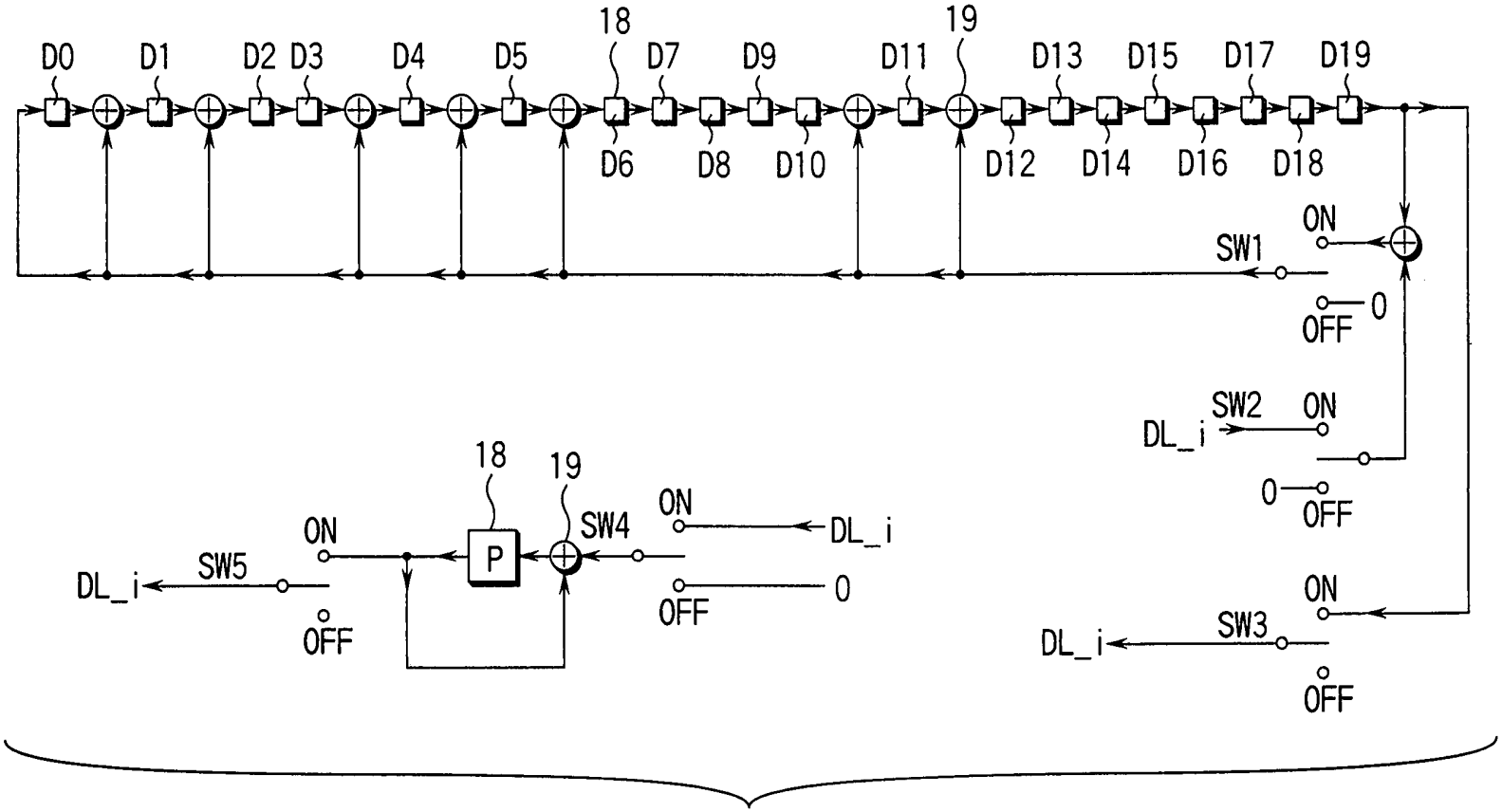

D0
D1
D2
D3
D4
D5
18
D7
D9
D11
19
D13
D15
D17
D19
D6
D8
D10
D12
D14
D16
D18
ON
SW1
OFF
0
SW2
ON
DL_i
0
OFF
18
19
ON
SW4
DL_i
ON
DL_i
SW5
P
OFF
0
OFF
ON
SW3
DL_i
OFF

FIG. 4

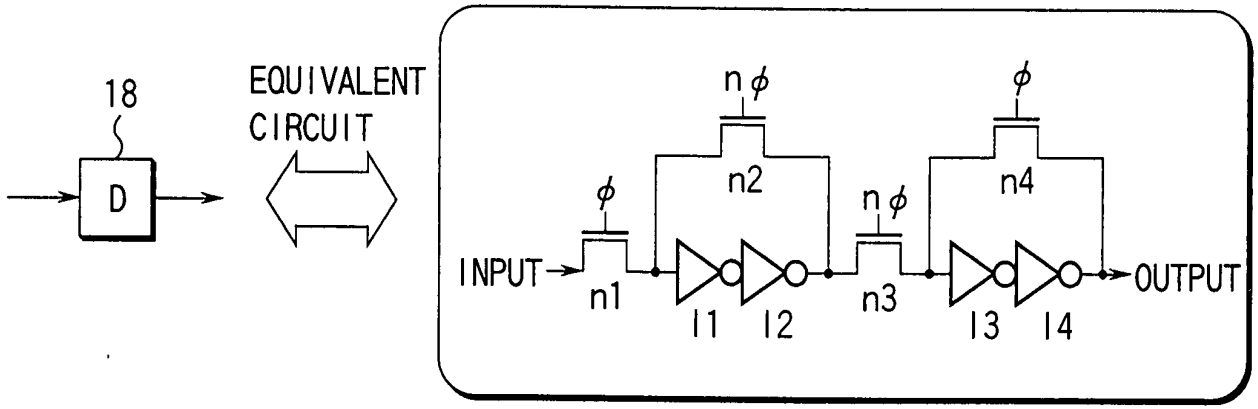
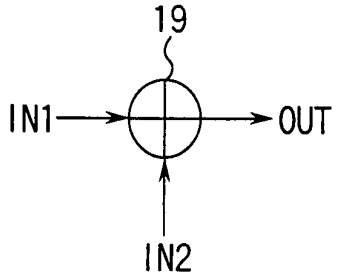



FIG. 5A




| IN1 | IN2 | OUT |
|---|---|---|
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

FIG. 5B

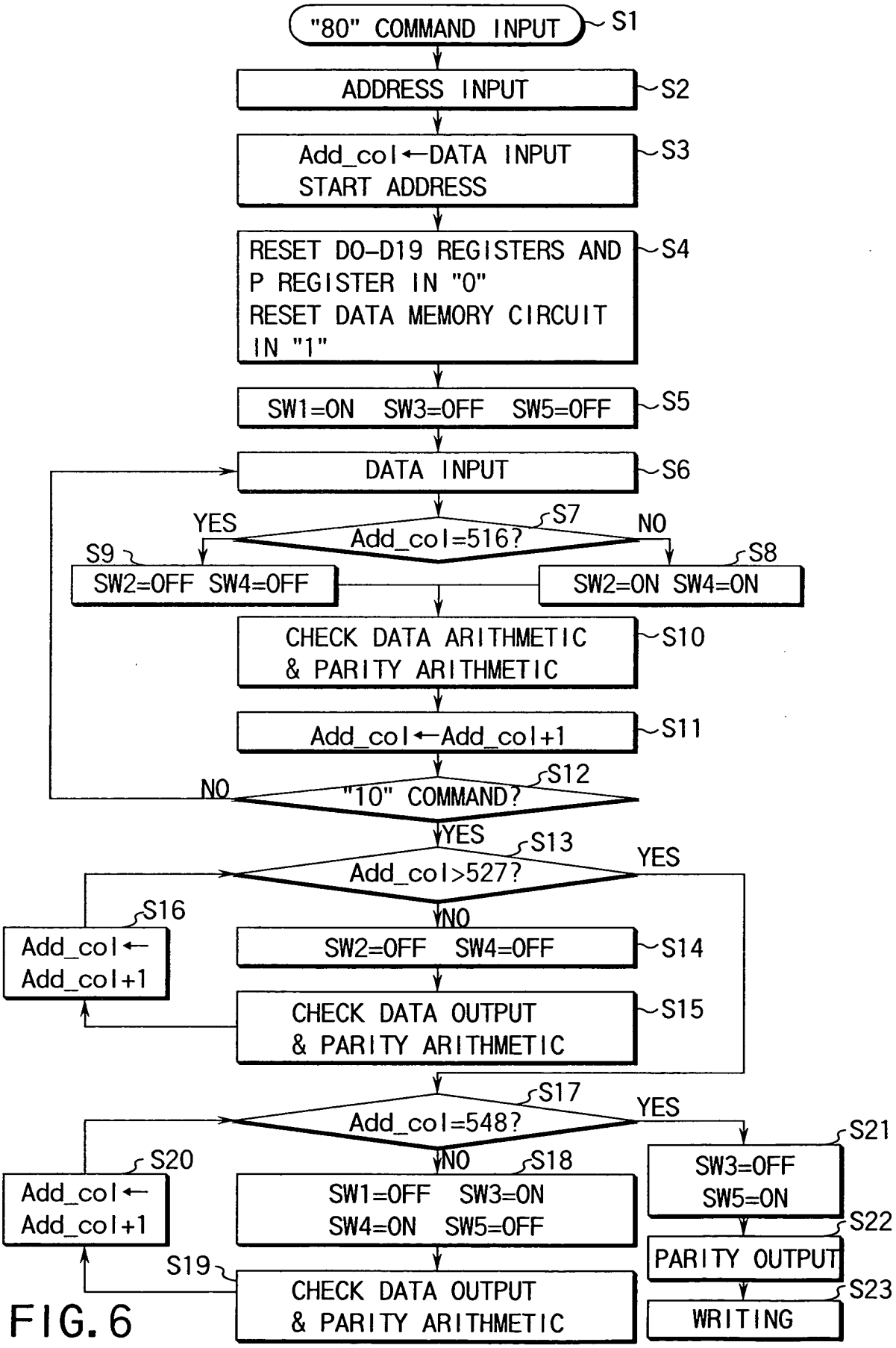

"80" COMMAND INPUT
S1
ADDRESS INPUT
S2
Add_col←DATA INPUT START ADDRESS
S3
RESET D0-D19 REGISTERS AND P REGISTER IN "0" RESET DATA MEMORY CIRCUIT IN "1"
S4
SW1=ON SW3=OFF SW5=OFF
S5
DATA INPUT
S6
Add_col=516?
S7
YES
NO
S9
SW2=OFF SW4=OFF
S8
SW2=ON SW4=ON
CHECK DATA ARITHMETIC & PARITY ARITHMETIC
S10
Add_col←Add_col+1
S11
"10" COMMAND?
S12
NO
YES
Add_col>527?
S13
YES
NO
S16
Add_col← Add_col+1
SW2=OFF SW4=OFF
S14
CHECK DATA OUTPUT & PARITY ARITHMETIC
S15
Add_col=548?
S17
YES
NO
S20
Add_col← Add_col+1
S18
SW1=OFF SW3=ON SW4=ON SW5=OFF
S19
CHECK DATA OUTPUT & PARITY ARITHMETIC
S21
SW3=OFF SW5=ON
S22
PARITY OUTPUT
S23
WRITING

FIG. 6

FIG. 7

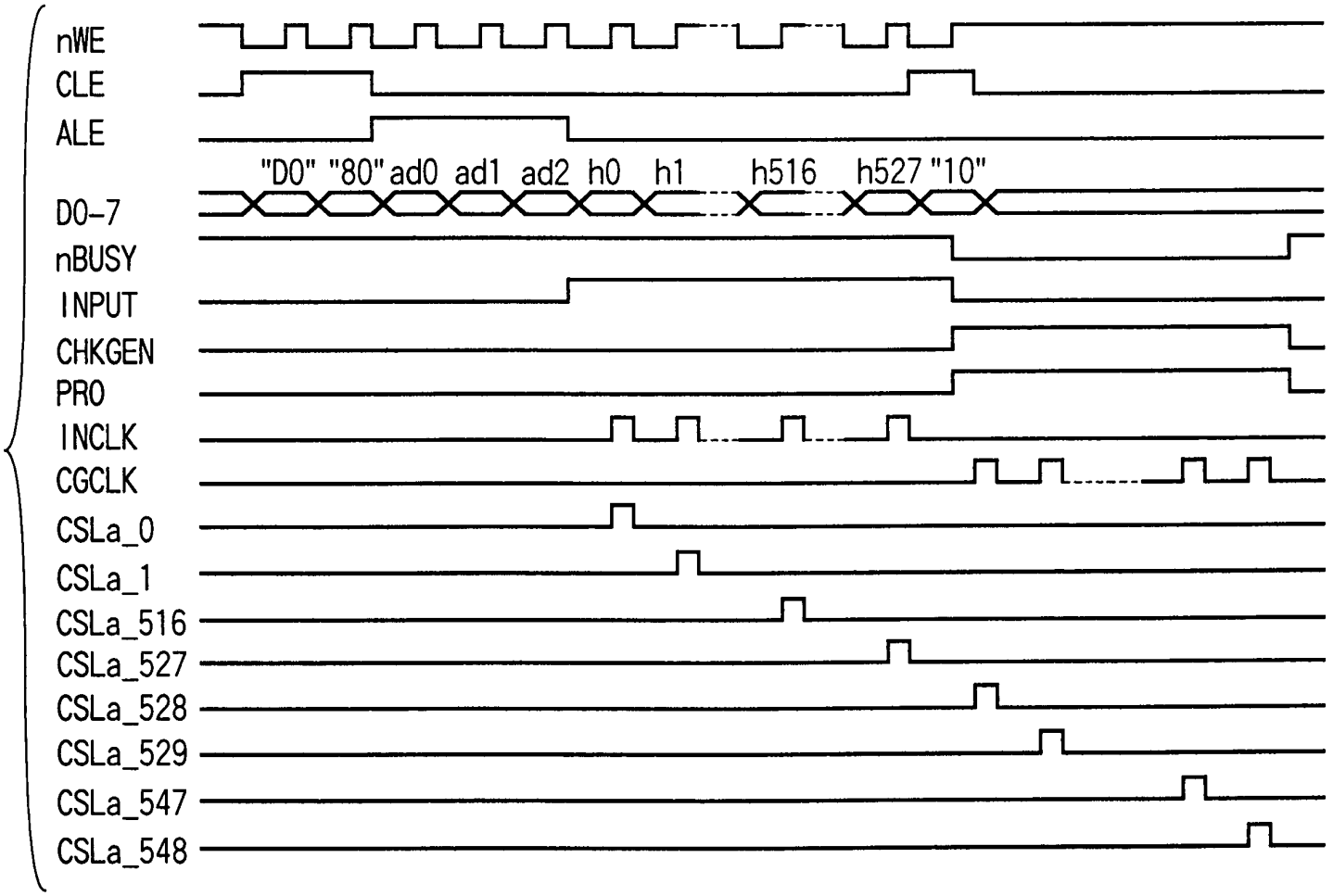

nWE
CLE
ALE
"D0" "80" ad0 ad1 ad2 h0 h1 h516 h527 "10"
D0-7
nBUSY
INPUT
CHKGEN
PRO
INCLK
CGCLK
CSLa_0
CSLa_1
CSLa_516
CSLa_527
CSLa_528
CSLa_529
CSLa_547
CSLa_548

FIG. 8

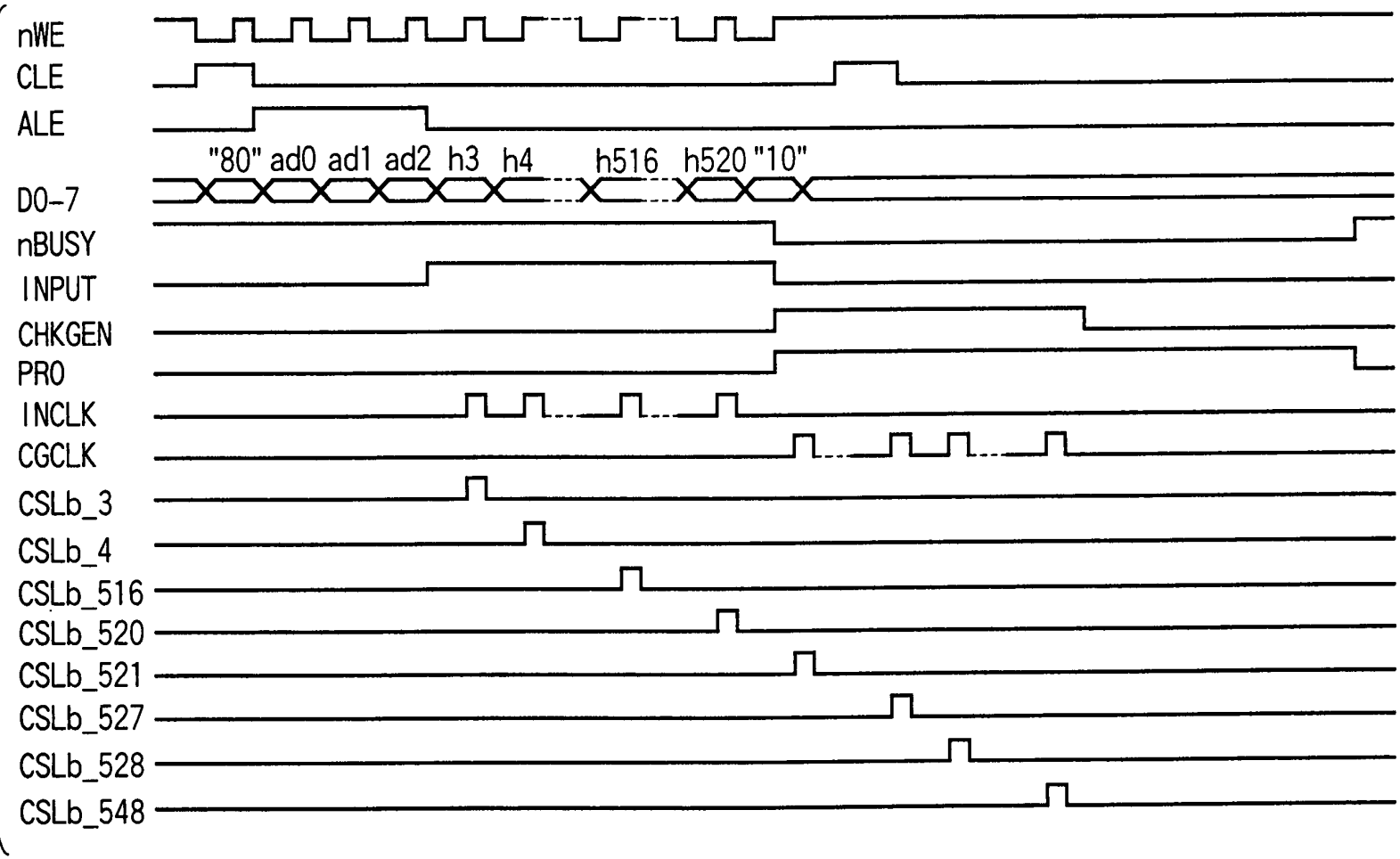

nWE
CLE
ALE
"80" ad0 ad1 ad2 h3 h4 h516 h520 "10"
D0-7
nBUSY
INPUT
CHKGEN
PRO
INCLK
CGCLK
CSLb_3
CSLb_4
CSLb_516
CSLb_520
CSLb_521
CSLb_527
CSLb_528
CSLb_548

FIG. 9

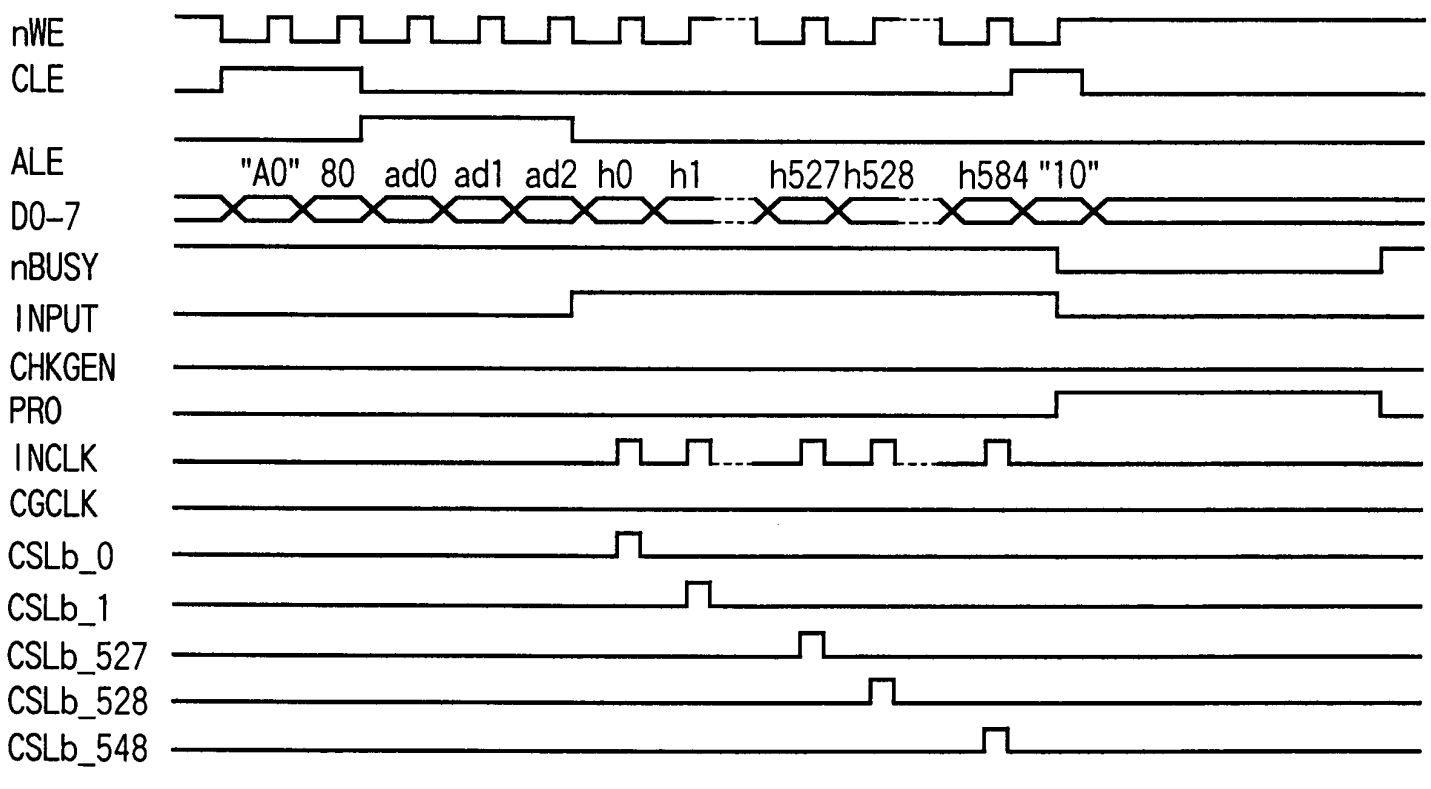
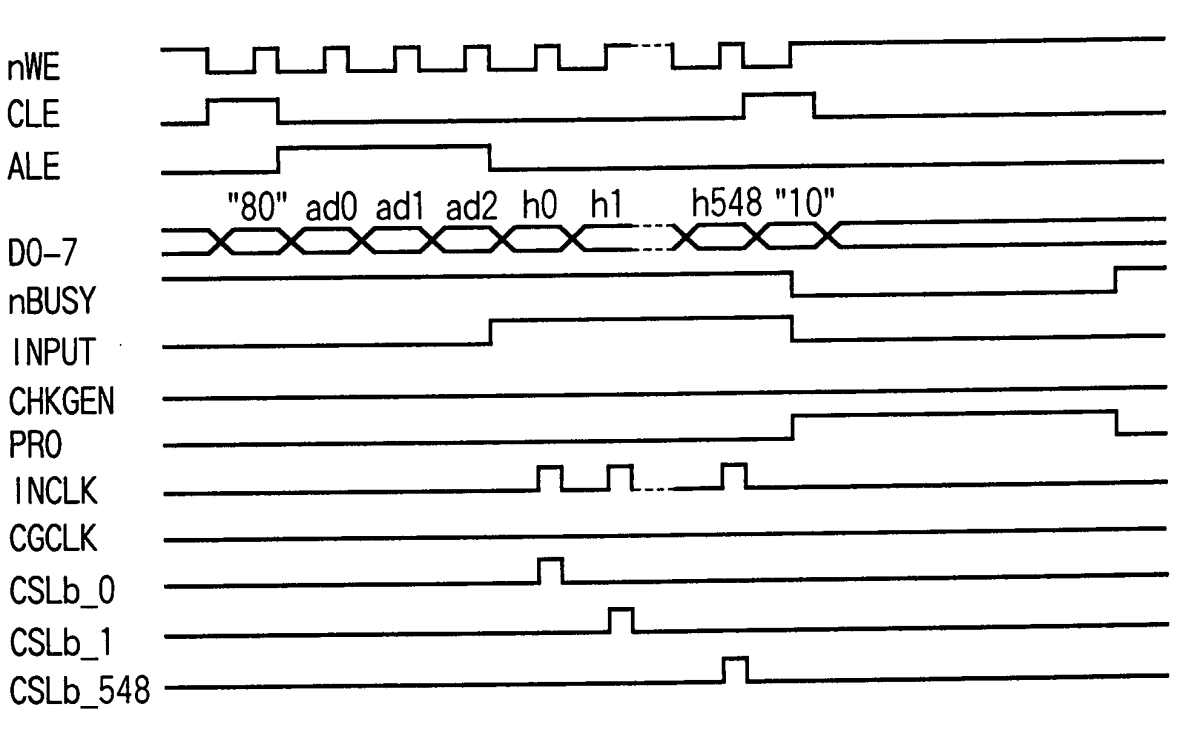

nWE
CLE
ALE
D0-7
nBUSY
INPUT
CHKGEN
PRO
INCLK
CGCLK
CSLb_0
CSLb_1
CSLb_527
CSLb_528
CSLb_548
"A0"
80
ad0
ad1
ad2
h0
h1
h527
h528
h584
"10"

FIG. 10


nWE
CLE
ALE
"80" ad0 ad1 ad2 h0 h1 h548 "10"
D0-7
nBUSY
INPUT
CHKGEN
PRO
INCLK
CGCLK
CSLb_0
CSLb_1
CSLb_548

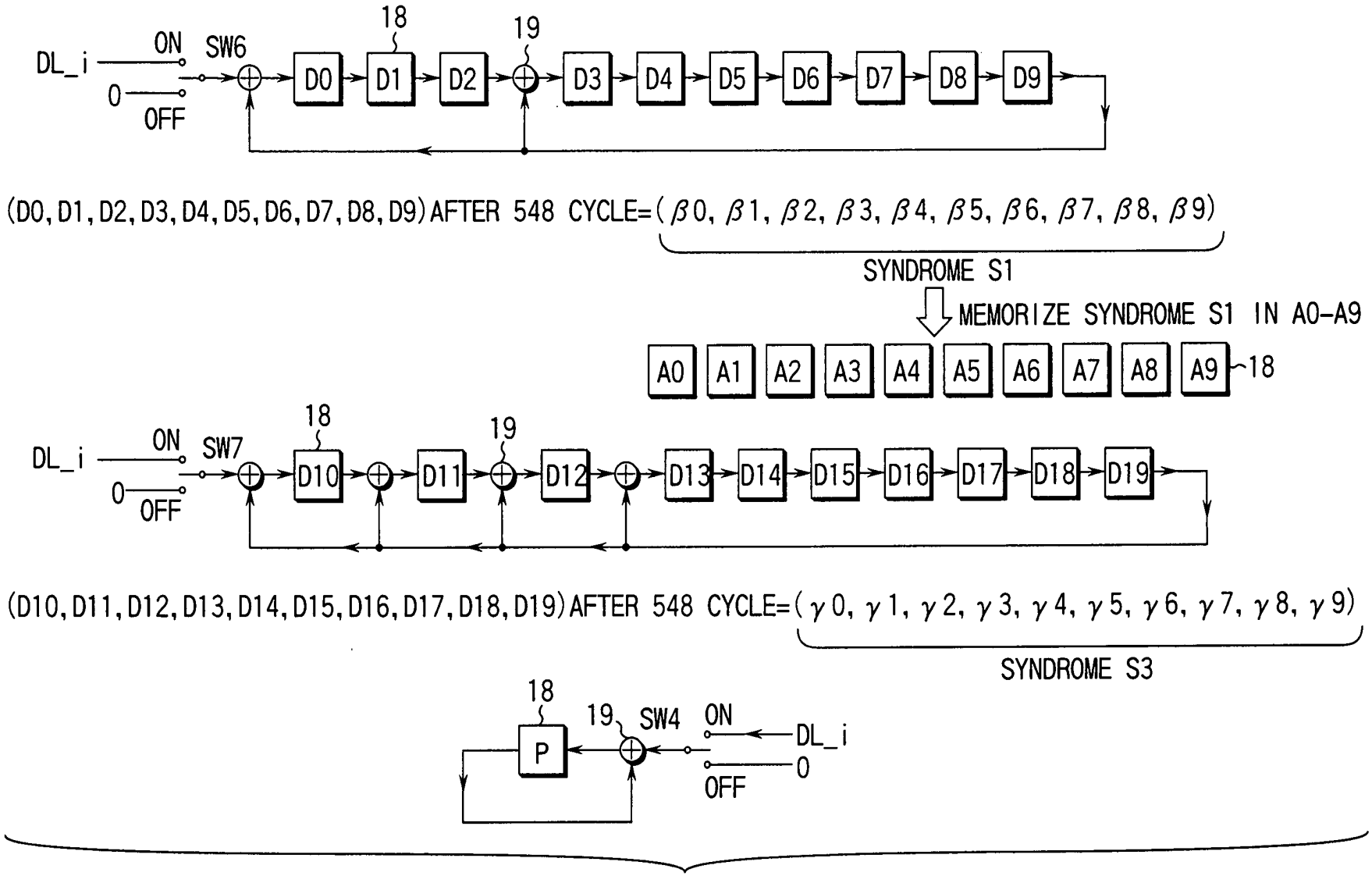
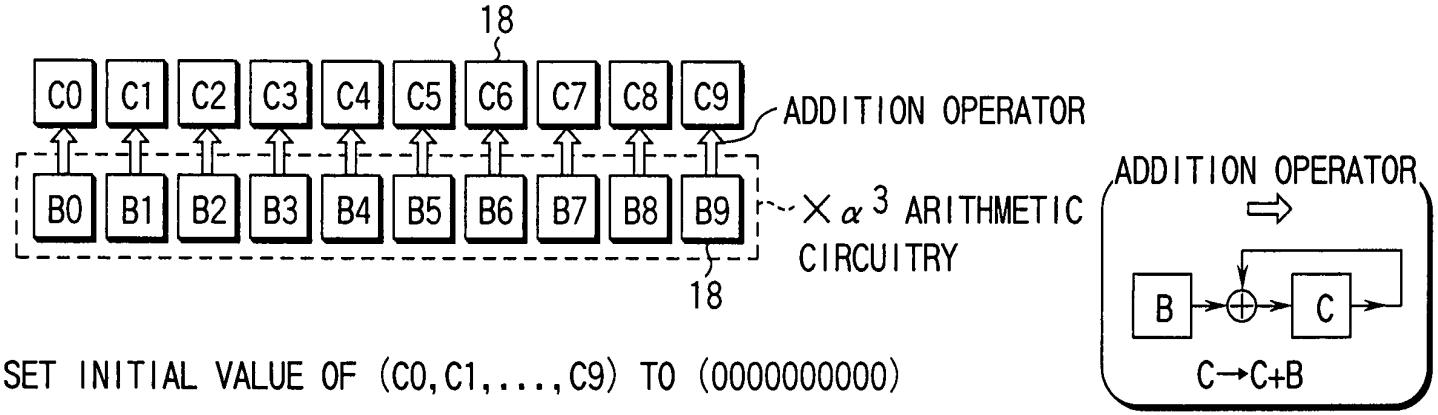

DL_i
ON
0
OFF
SW6
18
19
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
(D0, D1, D2, D3, D4, D5, D6, D7, D8, D9) AFTER 548 CYCLE=(β0, β1, β2, β3, β4, β5, β6, β7, β8, β9)
SYNDROME S1
MEMORIZE SYNDROME S1 IN A0-A9
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
18
DL_i
ON
0
OFF
SW7
18
19
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
(D10, D11, D12, D13, D14, D15, D16, D17, D18, D19) AFTER 548 CYCLE=(γ0, γ1, γ2, γ3, γ4, γ5, γ6, γ7, γ8, γ9)
SYNDROME S3
18
19
SW4
ON
OFF
DL_i
0
P

FIG. 11




STEP1 SET INITIAL VALUE OF (C0, C1, ..., C9) TO (0000000000)

STEP2 i=0~9 INPUT (B0, B1, ..., B9)=(1000000000) IS TO ×α3 ARITHMETIC CIRCUITRY AS INITIAL VALUE
IF γ1=1, PERFORM i CYCLES AND ADD B0 TO B9 TO C0 TO C9

END IF ADDITION FROM
i=0 TO i=9 IS COMPLETED

STEP3 FINAL VALUE OF (C0, C1, ..., C9)=
(δ0, δ1, ..., δ9)

⇩

VALUE OF (C0, C1, ..., C9)
IS LOADED TO (D0, D1, ..., D9)

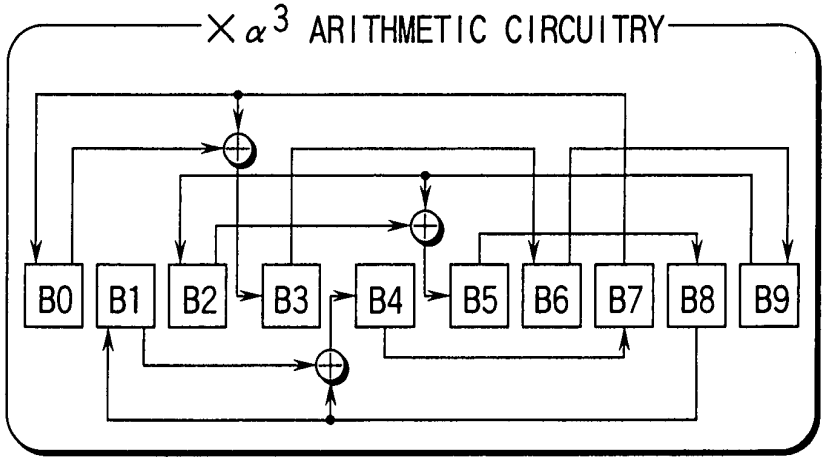



FIG. 12

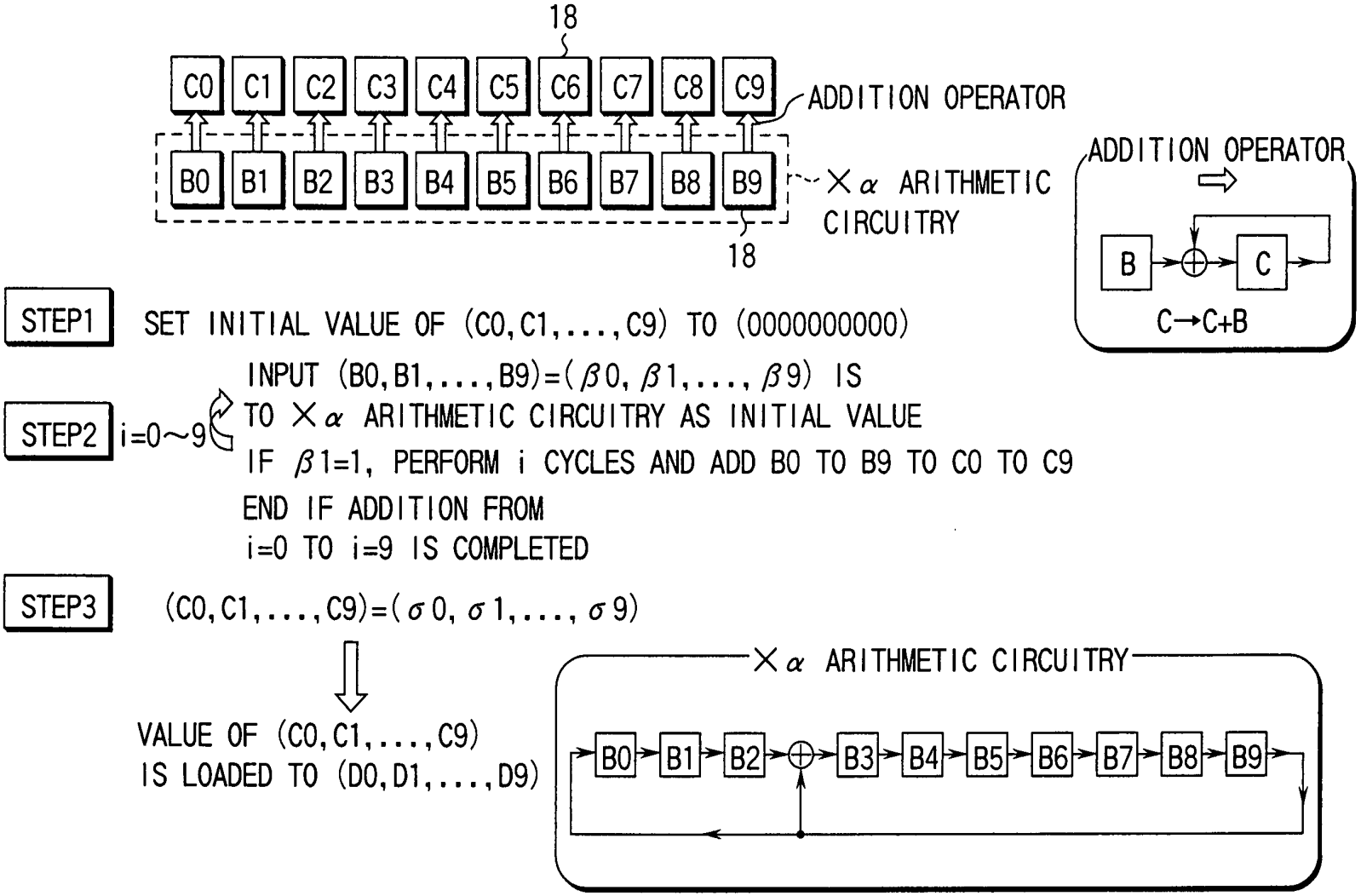

18
C0 C1 C2 C3 C4 C5 C6 C7 C8 C9
ADDITION OPERATOR
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9
×α ARITHMETIC CIRCUITRY
18
ADDITION OPERATOR
B
C
C→C+B
STEP1
SET INITIAL VALUE OF (C0,C1,...,C9) TO (0000000000)
STEP2
i=0~9
INPUT (B0,B1,...,B9)=(β0, β1,..., β9) IS
TO ×α ARITHMETIC CIRCUITRY AS INITIAL VALUE
IF β1=1, PERFORM i CYCLES AND ADD B0 TO B9 TO C0 TO C9
END IF ADDITION FROM
i=0 TO i=9 IS COMPLETED
STEP3
(C0,C1,...,C9)=(σ0, σ1,..., σ9)
VALUE OF (C0,C1,...,C9)
IS LOADED TO (D0,D1,...,D9)
×α ARITHMETIC CIRCUITRY
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9

FIG. 13

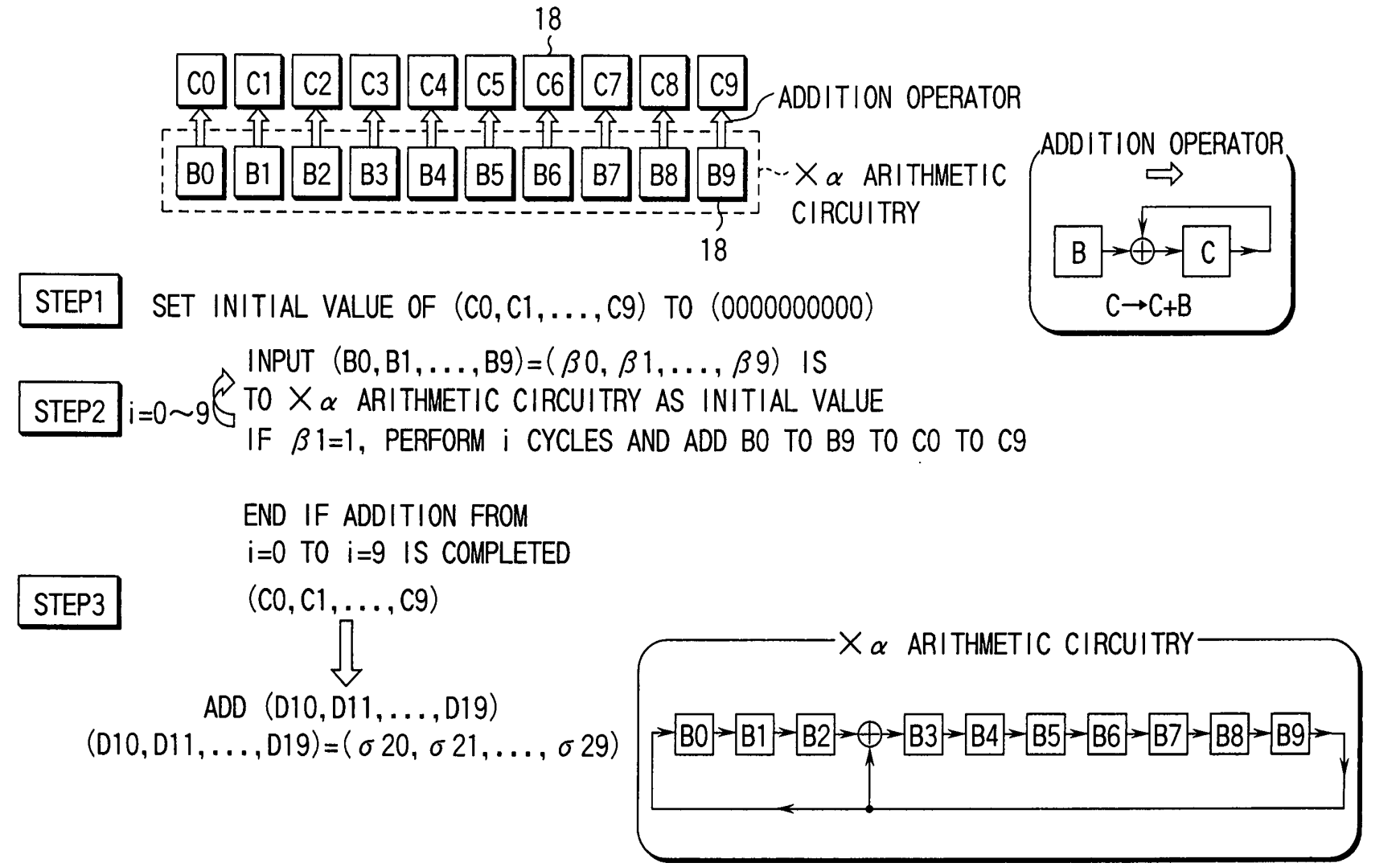
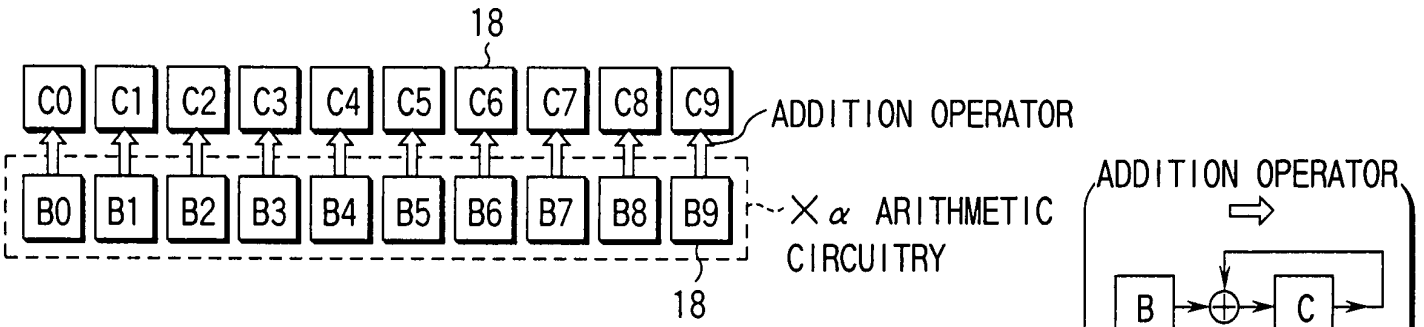
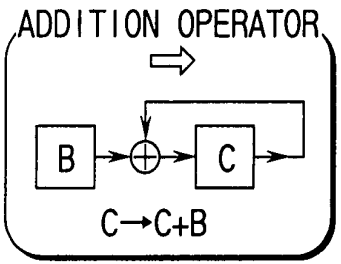

18
C0 C1 C2 C3 C4 C5 C6 C7 C8 C9
ADDITION OPERATOR
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9
×α ARITHMETIC CIRCUITRY
18
ADDITION OPERATOR
B
C
C→C+B
STEP1
SET INITIAL VALUE OF (C0,C1,...,C9) TO (0000000000)
STEP2
i=0~9
INPUT (B0,B1,...,B9)=(β0, β1,..., β9) IS TO ×α ARITHMETIC CIRCUITRY AS INITIAL VALUE
IF β1=1, PERFORM i CYCLES AND ADD B0 TO B9 TO C0 TO C9
END IF ADDITION FROM i=0 TO i=9 IS COMPLETED
STEP3
(C0,C1,...,C9)
ADD (D10,D11,...,D19)
(D10,D11,...,D19)=(σ20, σ21,..., σ29)
×α ARITHMETIC CIRCUITRY
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9

FIG. 14




STEP1 SET INITIAL VALUE OF (C0,C1,...,C9) TO (0000000000)

STEP2 i=0~9

INPUT (B0,B1,...,B9)=(1010001111) IS
TO ×α ARITHMETIC CIRCUITRY AS INITIAL VALUE
IF σ1i=1, PERFORM i CYCLES AND ADD B0 TO B9 TO C0 TO C9

END IF ADDITION FROM
i=0 TO i=9 IS COMPLETED

STEP3 (C10,C11,...,C19)=(σ10, σ11,..., σ19)×α 457

VALUE OF (C10,C11,...,C19) IS LOADED TO
(D10,D11,...,D19)
(D0,D1,...,D9)=(λ10, λ11,..., λ19)

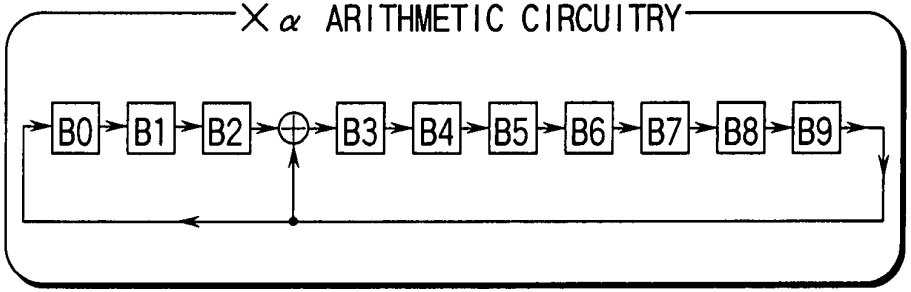



FIG. 15

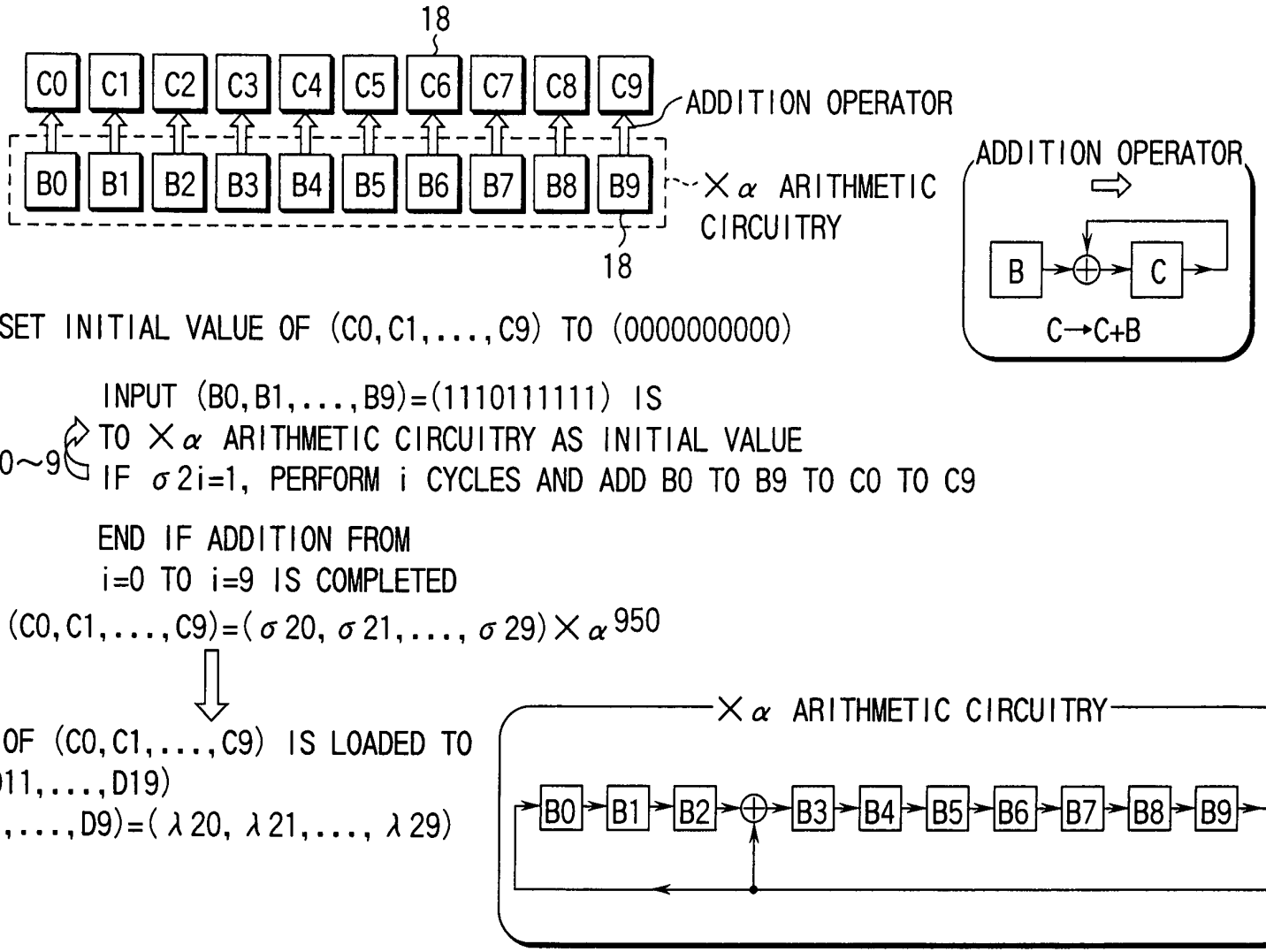
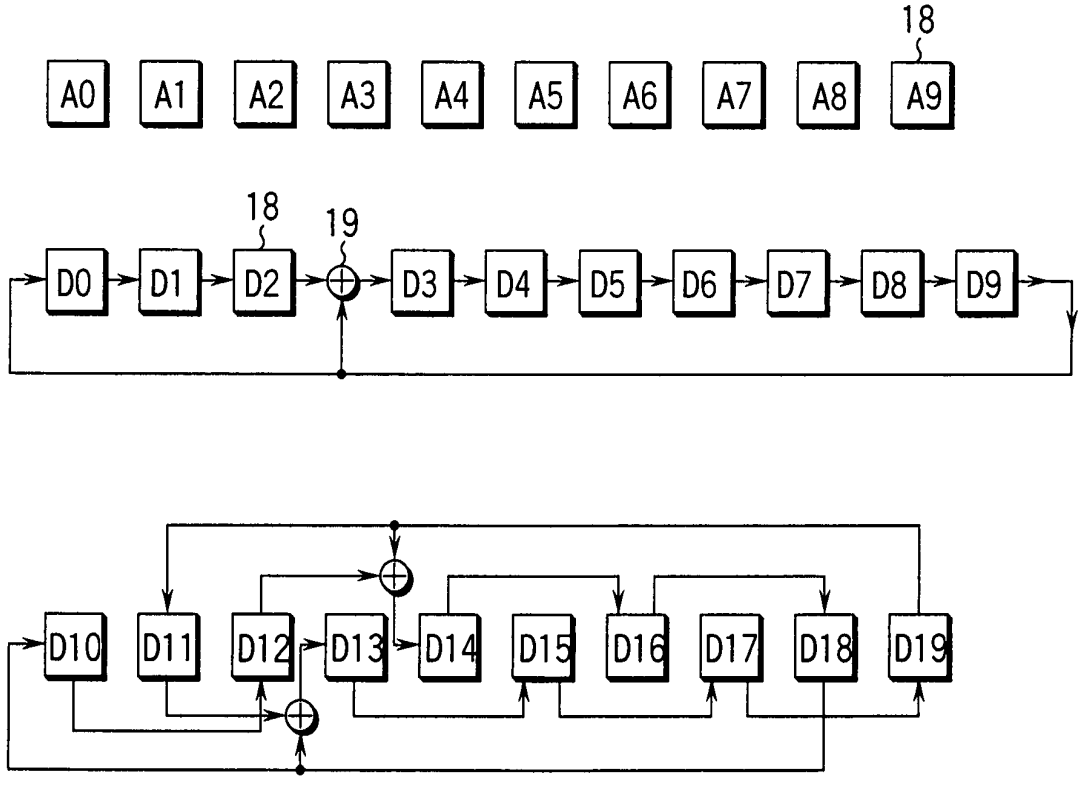

18
C0 C1 C2 C3 C4 C5 C6 C7 C8 C9
ADDITION OPERATOR
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9
×α ARITHMETIC CIRCUITRY
18
ADDITION OPERATOR
B
C
C→C+B
STEP1
SET INITIAL VALUE OF (C0,C1,...,C9) TO (0000000000)
INPUT (B0,B1,...,B9)=(1110111111) IS
TO ×α ARITHMETIC CIRCUITRY AS INITIAL VALUE
STEP2
i=0~9
IF σ2i=1, PERFORM i CYCLES AND ADD B0 TO B9 TO C0 TO C9
END IF ADDITION FROM
i=0 TO i=9 IS COMPLETED
STEP3
(C0,C1,...,C9)=(σ20, σ21,..., σ29)×α950
VALUE OF (C0,C1,...,C9) IS LOADED TO
(D10,D11,...,D19)
(D0,D1,...,D9)=(λ20, λ21,..., λ29)
×α ARITHMETIC CIRCUITRY
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9

FIG. 16

FIG. 17


18
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
18
19
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19

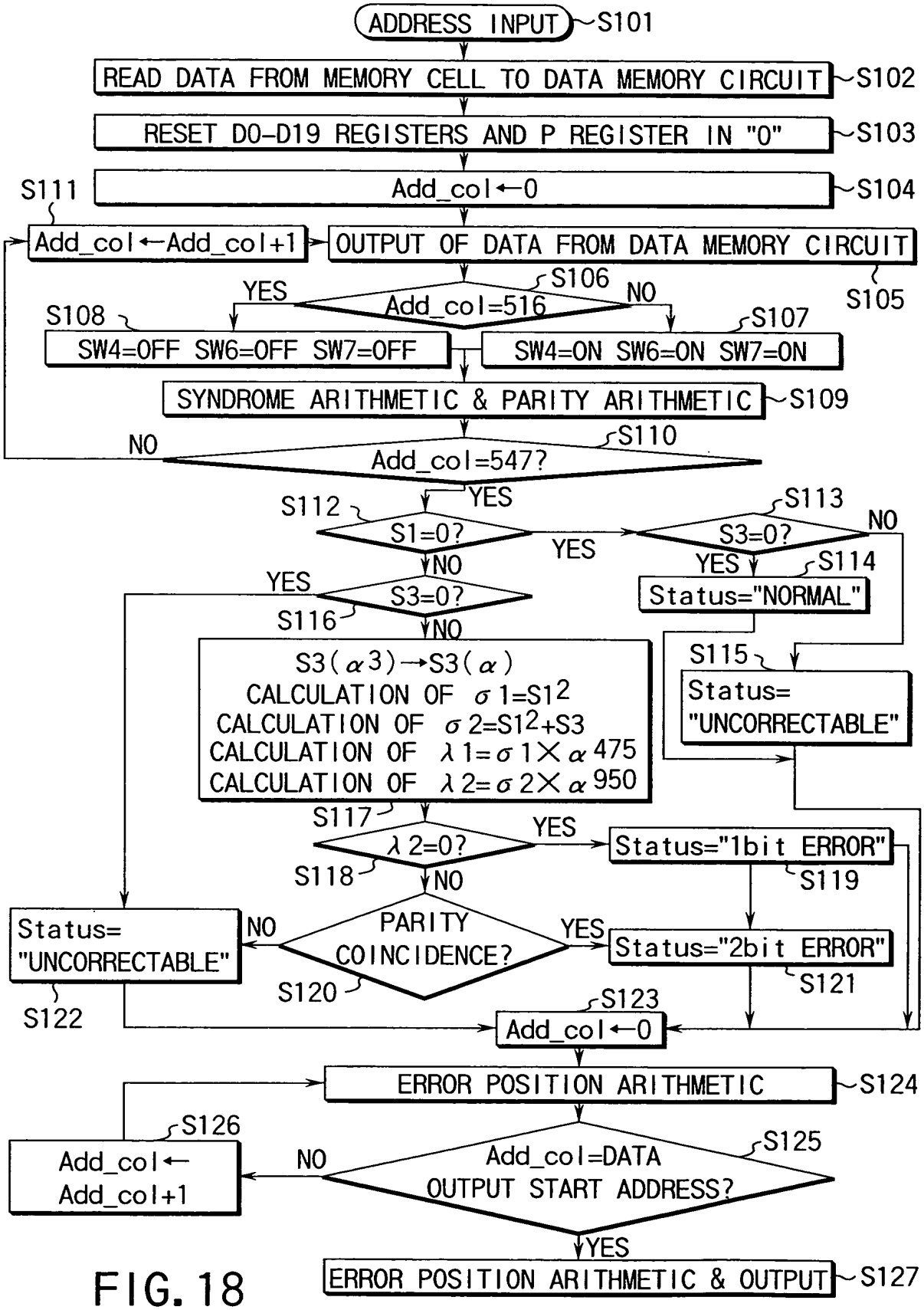

ADDRESS INPUT
S101
READ DATA FROM MEMORY CELL TO DATA MEMORY CIRCUIT
S102
RESET D0-D19 REGISTERS AND P REGISTER IN "0"
S103
Add_col←0
S104
S111
Add_col←Add_col+1
OUTPUT OF DATA FROM DATA MEMORY CIRCUIT
S105
S106
Add_col=516
YES
NO
S108
SW4=OFF SW6=OFF SW7=OFF
S107
SW4=ON SW6=ON SW7=ON
SYNDROME ARITHMETIC & PARITY ARITHMETIC
S109
S110
Add_col=547?
NO
YES
S112
S1=0?
YES
S113
S3=0?
NO
YES
S114
Status="NORMAL"
NO
YES
S3=0?
S116
NO
S3(α3)→S3(α)
CALCULATION OF σ1=S1²
CALCULATION OF σ2=S1²+S3
CALCULATION OF λ1=σ1×α475
CALCULATION OF λ2=σ2×α950
S115
Status=
"UNCORRECTABLE"
S117
λ2=0?
YES
Status="1bit ERROR"
S119
S118
NO
PARITY
COINCIDENCE?
NO
YES
Status=
"UNCORRECTABLE"
S120
Status="2bit ERROR"
S121
S122
S123
Add_col←0
ERROR POSITION ARITHMETIC
S124
S126
Add_col←
Add_col+1
NO
Add_col=DATA
OUTPUT START ADDRESS?
S125
YES
ERROR POSITION ARITHMETIC & OUTPUT
S127

FIG. 18

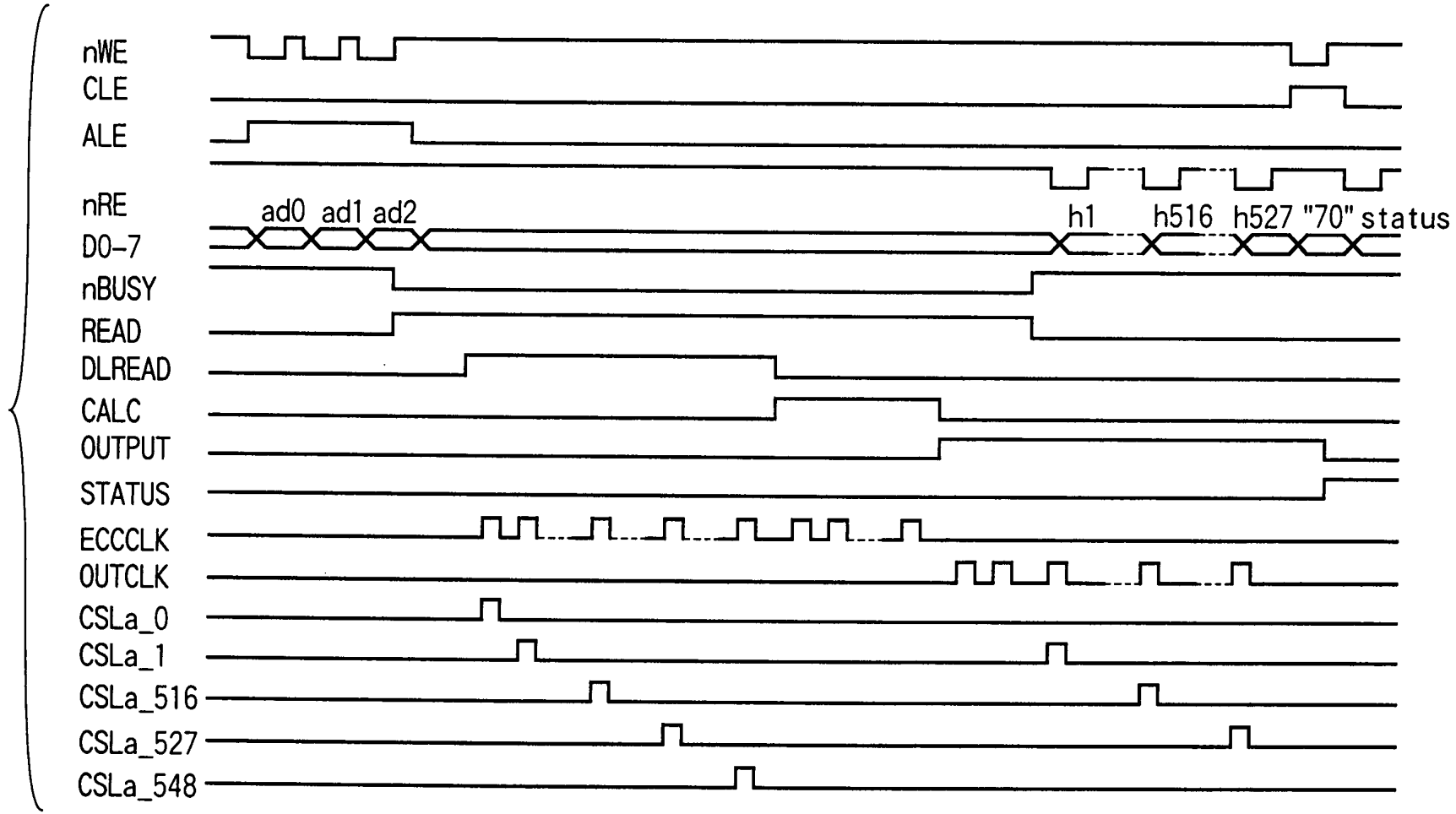

nWE
CLE
ALE
nRE
D0-7
nBUSY
READ
DLREAD
CALC
OUTPUT
STATUS
ECCCLK
OUTCLK
CSLa_0
CSLa_1
CSLa_516
CSLa_527
CSLa_548
ad0 ad1 ad2
h1
h516
h527
"70"
status

FIG. 19

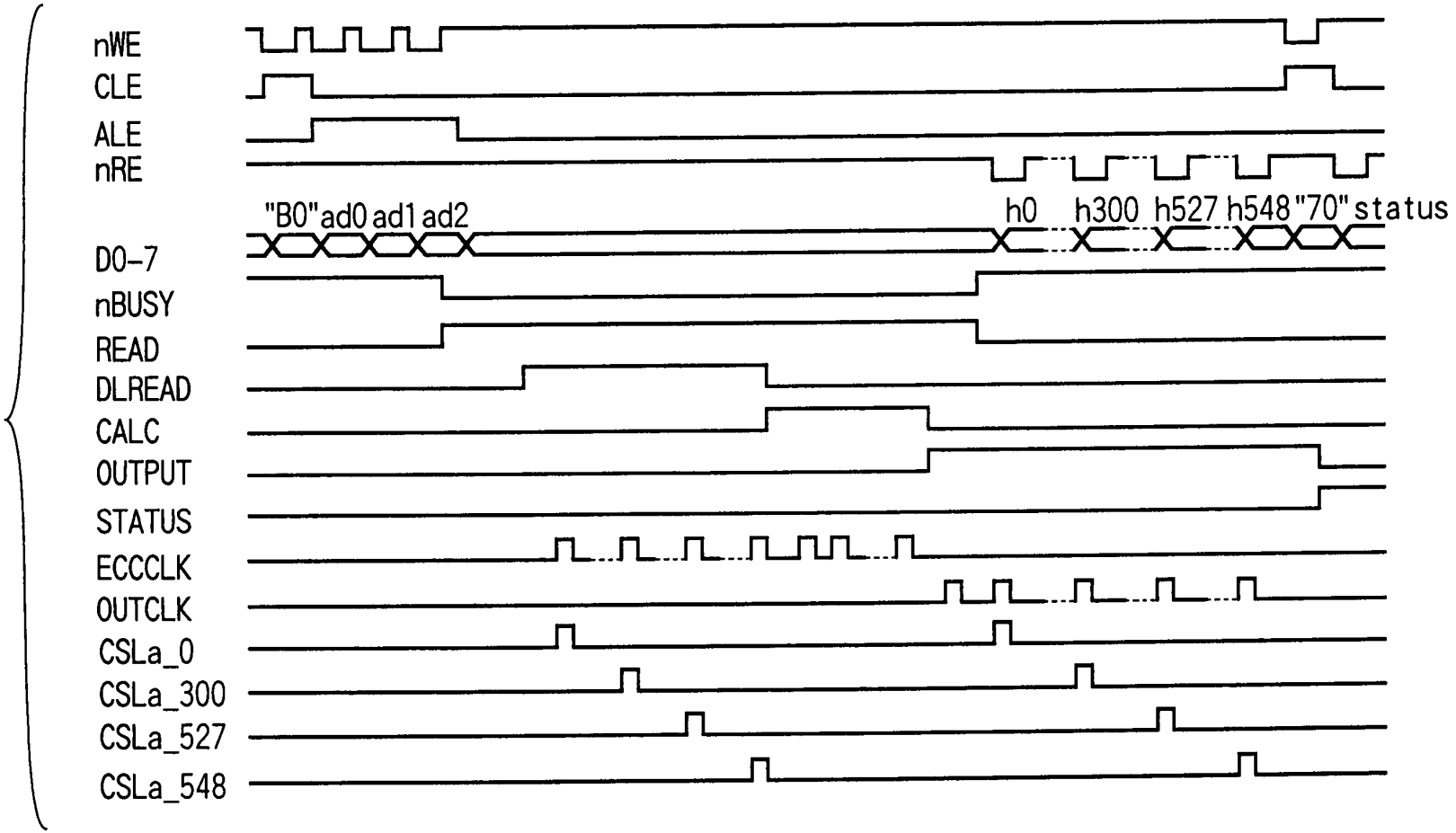

nWE
CLE
ALE
nRE
"B0" ad0 ad1 ad2
h0
h300
h527
h548
"70"
status
D0-7
nBUSY
READ
DLREAD
CALC
OUTPUT
STATUS
ECCCLK
OUTCLK
CSLa_0
CSLa_300
CSLa_527
CSLa_548

FIG. 20

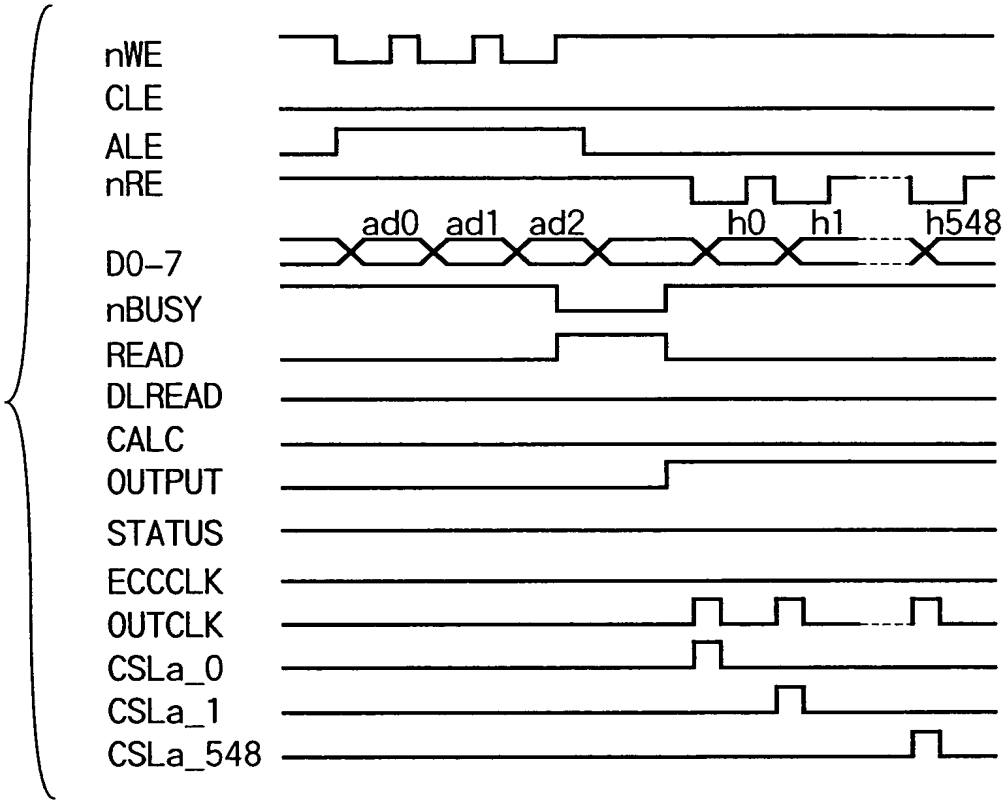

nWE
CLE
ALE
nRE
ad0
ad1
ad2
h0
h1
h548
D0-7
nBUSY
READ
DLREAD
CALC
OUTPUT
STATUS
ECCCLK
OUTCLK
CSLa_0
CSLa_1
CSLa_548

FIG. 21

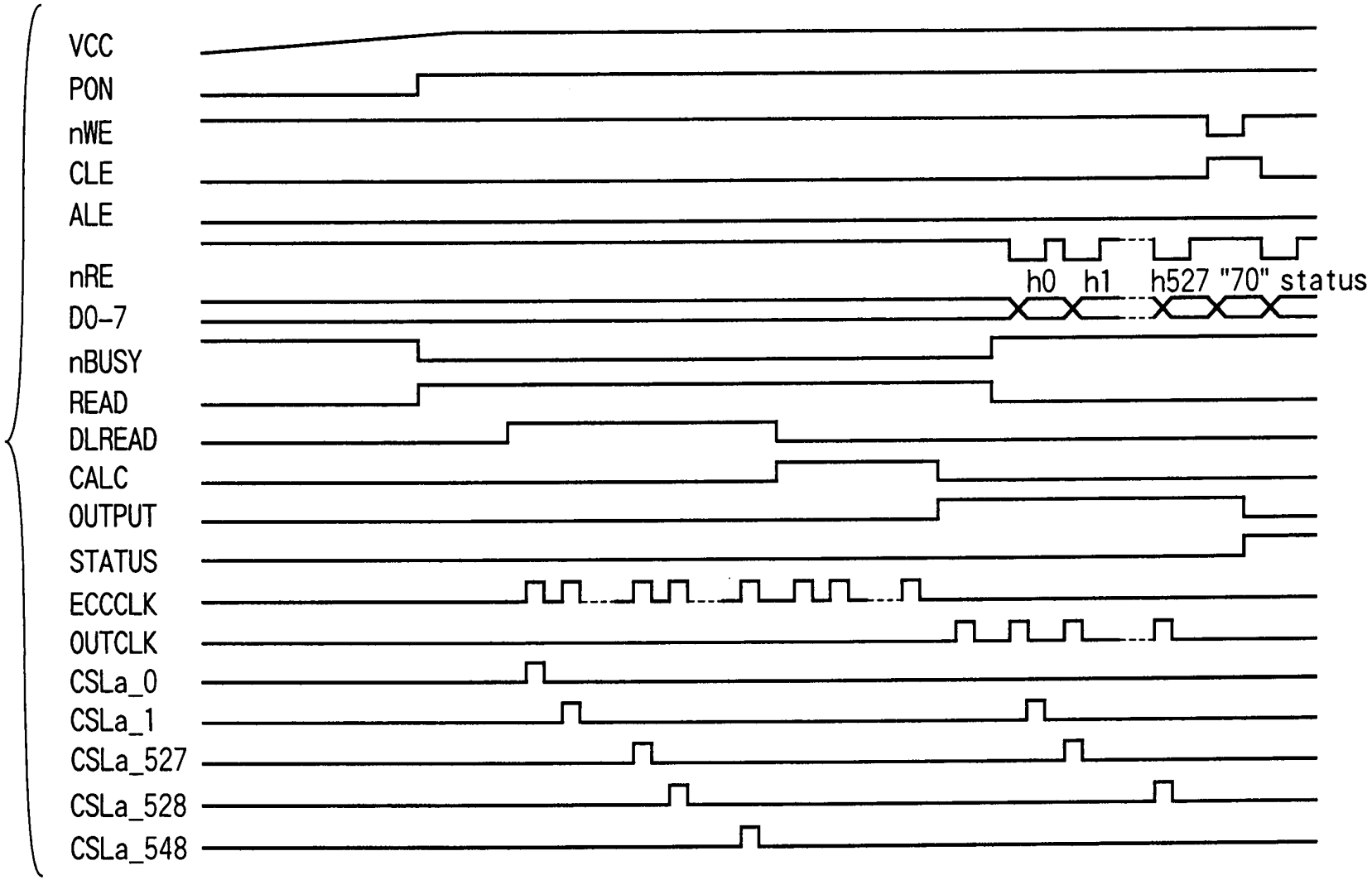

VCC
PON
nWE
CLE
ALE
nRE
h0 h1 h527 "70" status
D0-7
nBUSY
READ
DLREAD
CALC
OUTPUT
STATUS
ECCCLK
OUTCLK
CSLa_0
CSLa_1
CSLa_527
CSLa_528
CSLa_548

FIG. 22

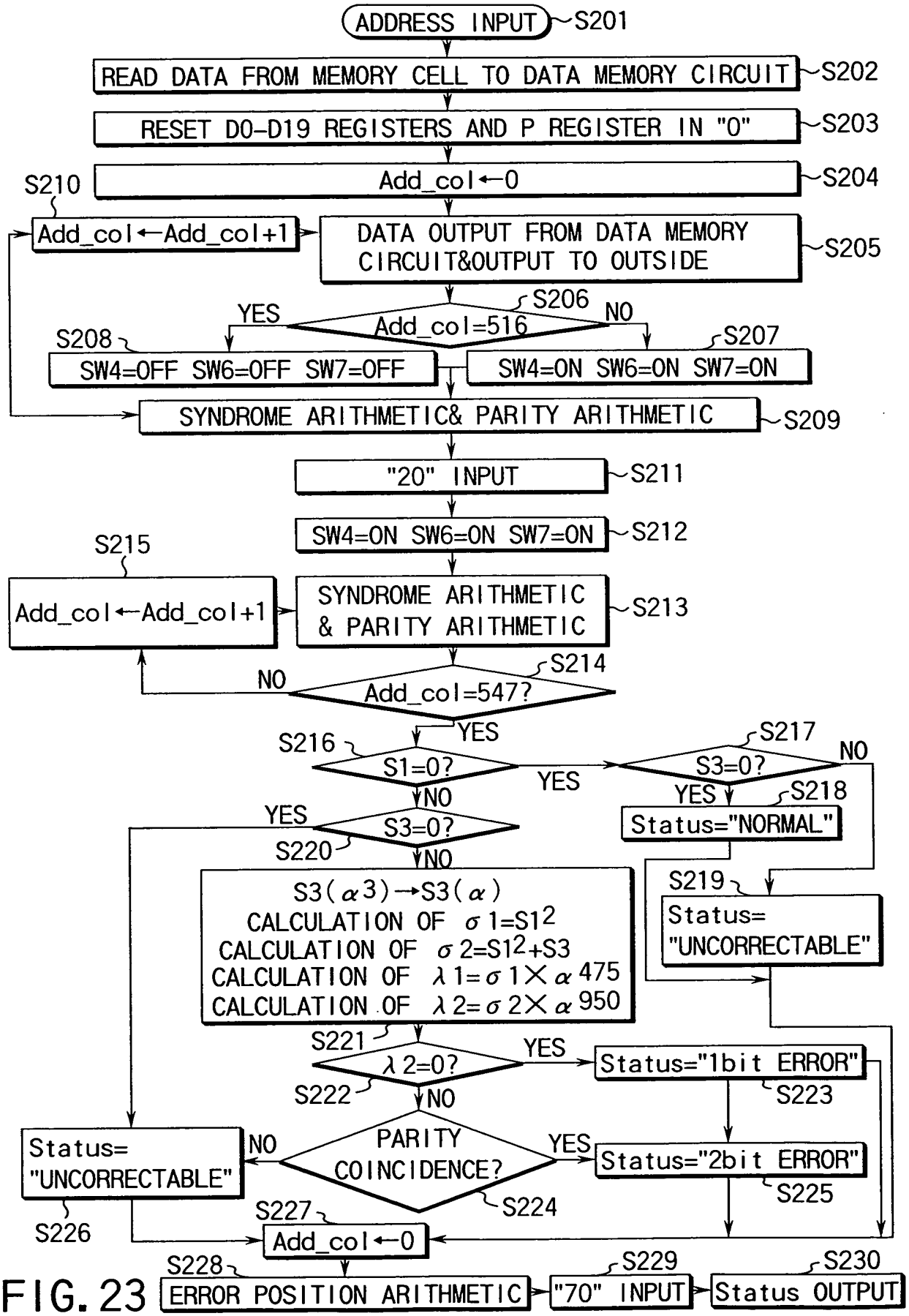
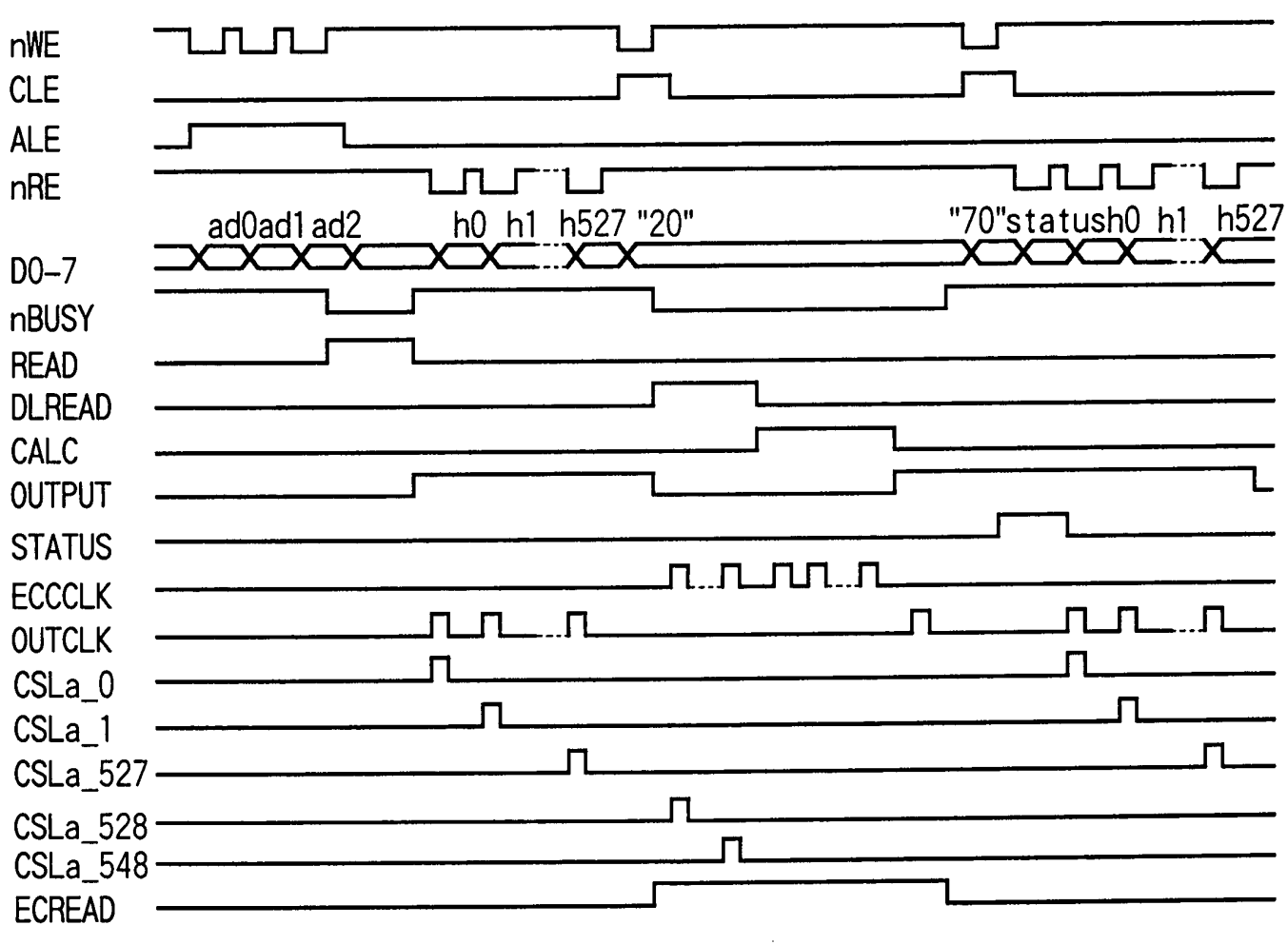

ADDRESS INPUT
S201
READ DATA FROM MEMORY CELL TO DATA MEMORY CIRCUIT
S202
RESET D0-D19 REGISTERS AND P REGISTER IN "0"
S203
Add_col←0
S204
S210
Add_col←Add_col+1
DATA OUTPUT FROM DATA MEMORY CIRCUIT&OUTPUT TO OUTSIDE
S205
S206
YES
Add_col=516
NO
S208
S207
SW4=0FF SW6=0FF SW7=0FF
SW4=ON SW6=ON SW7=ON
SYNDROME ARITHMETIC& PARITY ARITHMETIC
S209
"20" INPUT
S211
SW4=ON SW6=ON SW7=ON
S212
S215
Add_col←Add_col+1
SYNDROME ARITHMETIC & PARITY ARITHMETIC
S213
S214
NO
Add_col=547?
YES
S216
S1=0?
YES
S217
S3=0?
NO
YES
S218
Status="NORMAL"
YES
S3=0?
S220
NO
S219
S3(α3)→S3(α)
CALCULATION OF σ1=S1²
CALCULATION OF σ2=S1²+S3
CALCULATION OF λ1=σ1×α475
CALCULATION OF λ2=σ2×α950
Status= "UNCORRECTABLE"
S221
λ2=0?
YES
Status="1bit ERROR"
S222
S223
NO
Status= "UNCORRECTABLE"
NO
PARITY COINCIDENCE?
YES
Status="2bit ERROR"
S224
S225
S226
S227
Add_col←0
S228
ERROR POSITION ARITHMETIC
S229
"70" INPUT
S230
Status OUTPUT

FIG. 23

FIG. 24


nWE
CLE
ALE
nRE
ad0ad1 ad2
h0 h1 h527 "20"
"70"statush0 h1 h527
D0-7
nBUSY
READ
DLREAD
CALC
OUTPUT
STATUS
ECCCLK
OUTCLK
CSLa_0
CSLa_1
CSLa_527
CSLa_528
CSLa_548
ECREAD

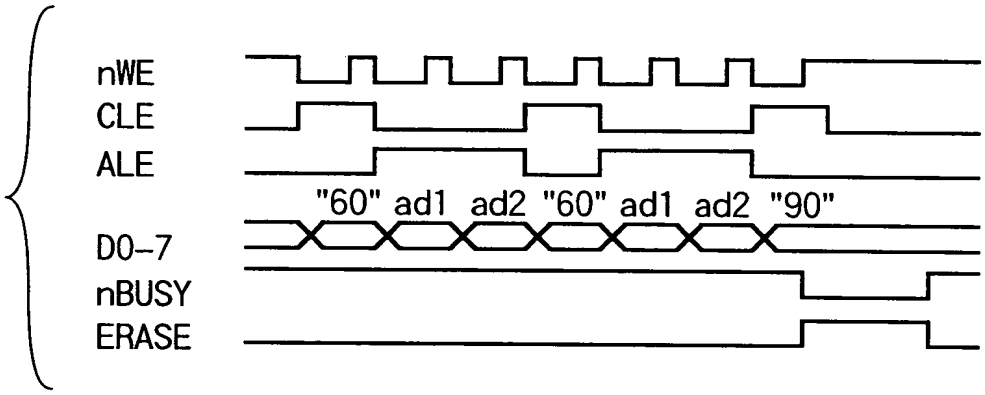



FIG. 25